# DATA SHEET

# TDA8766
## 10-bit high-speed 3.0 to 5.25 V analog-to-digital converter

Product specification
Supersedes data of 2001 Apr 19

2002 Jul 02

Philips
Semiconductors




PHILIPS

# 10-bit high-speed 3.0 to 5.25 V analog-to-digital converter

# TDA8766

## FEATURES

- 10-bit resolution
- 3.0 to 5.25 V operation
- Sampling rate up to 20 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 1.0 MHz; full-scale input at $f_{clk}$ = 20 MHz)
- In-Range (IR) CMOS output
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 53 mW (typical value)
- Low analog input capacitance, no buffer amplifier required
- Standby mode
- No sample-and-hold circuit required.

## APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Camera
- Camcorder
- Radio communication.

## GENERAL DESCRIPTION

The TDA8766 is a 10-bit high-speed Analog-to-Digital Converter (ADC) for professional video and other applications. It converts with 3.0 to 5.25 V operation the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 20 MHz. All digital inputs and outputs are CMOS compatible. A standby mode allows reduction of the device power consumption down to 4 mW.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | analog supply voltage | | 3.0 | 3.3 | 5.25 | V |
| $V_{DDD1}$ | digital supply voltage 1 | | 3.0 | 3.3 | 5.25 | V |
| $V_{DDD2}$ | digital supply voltage 2 | | 3.0 | 3.3 | 5.25 | V |
| $V_{DDO}$ | output stages supply voltage | | 3.0 | 3.3 | 5.25 | V |
| $I_{DDA}$ | analog supply current | | – | 7.5 | 10 | mA |
| $I_{DDD}$ | digital supply current | | – | 7.5 | 10 | mA |
| $I_{DDO}$ | output stages supply current | $f_{clk}$ = 20 MHz; $C_L$ = 20 pF; ramp input | – | 1 | 2 | mA |
| INL | integral non-linearity | $f_{clk}$ = 20 MHz; ramp input | – | ±1 | ±2 | LSB |
| DNL | differential non-linearity | $f_{clk}$ = 20 MHz; ramp input | – | ±0.25 | ±0.7 | LSB |
| $f_{clk(max)}$ | maximum clock frequency | | 20 | – | – | MHz |
| $P_{tot}$ | total power dissipation | $V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V | – | 53 | 73 | mW |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA8766G | LQFP32 | plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm | SOT401-1 |

## BLOCK DIAGRAM

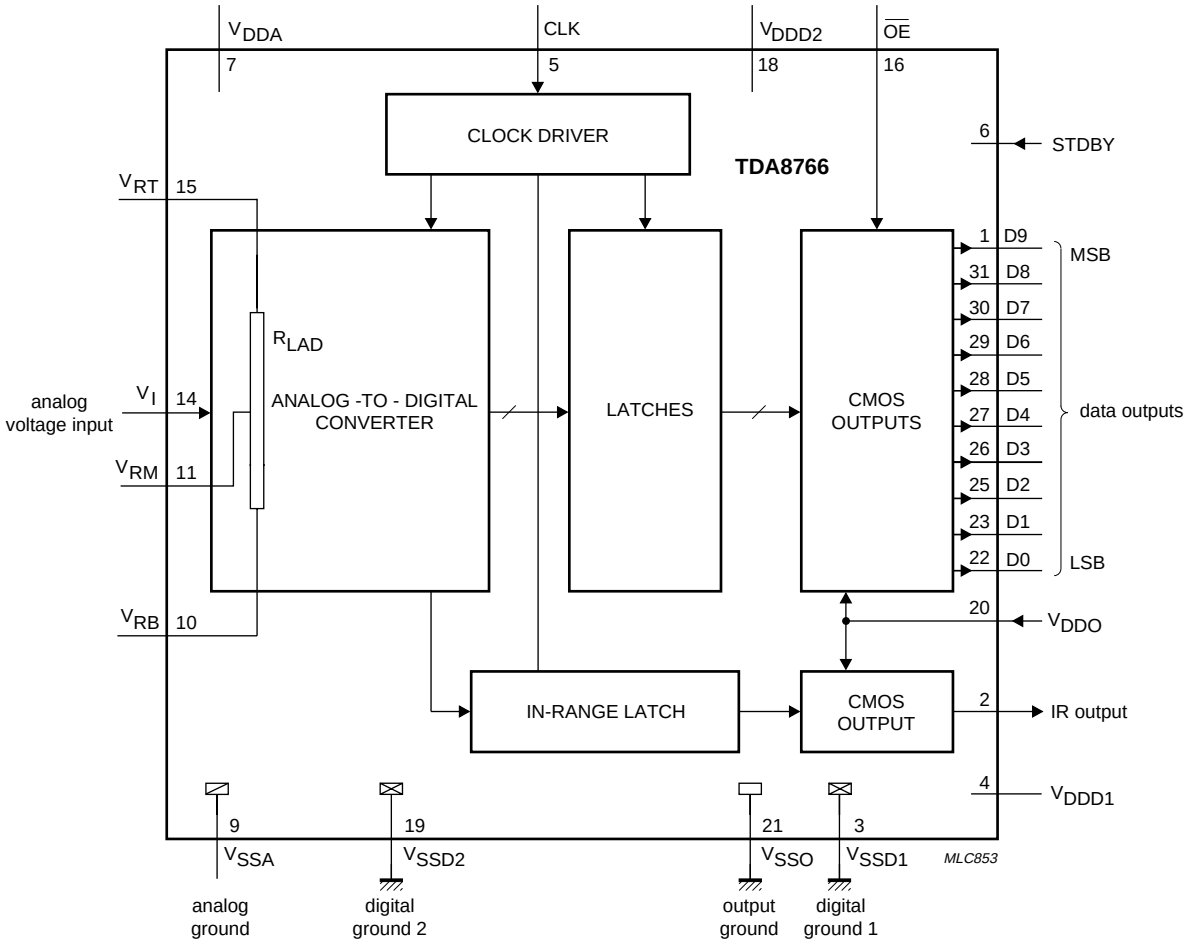



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| D9 | 1 | data output; bit 9 (MSB) |
| IR | 2 | in-range data output |
| $V_{SSD1}$ | 3 | digital ground 1 |
| $V_{DDD1}$ | 4 | digital supply voltage 1 (3.0 to 5.25 V) |
| CLK | 5 | clock input |
| STDBY | 6 | standby mode input |
| $V_{DDA}$ | 7 | analog supply voltage (3.0 to 5.25 V) |
| n.c. | 8 | not connected |
| $V_{SSA}$ | 9 | analog ground |
| $V_{RB}$ | 10 | reference voltage BOTTOM input |
| $V_{RM}$ | 11 | reference voltage MIDDLE input |
| n.c. | 12 | not connected |
| n.c. | 13 | not connected |
| $V_I$ | 14 | analog voltage input |
| $V_{RT}$ | 15 | reference voltage TOP input |
| $\overline{OE}$ | 16 | output enable input (active LOW) |
| n.c. | 17 | not connected |
| $V_{DDD2}$ | 18 | digital supply voltage 2 (3.0 to 5.25 V) |
| $V_{SSD2}$ | 19 | digital ground 2 |
| $V_{DDO}$ | 20 | positive supply voltage for output stage (3.0 to 5.25 V) |
| $V_{SSO}$ | 21 | output stage ground |
| D0 | 22 | data output; bit 0 (LSB) |
| D1 | 23 | data output; bit 1 |
| n.c. | 24 | not connected |
| D2 | 25 | data output; bit 2 |
| D3 | 26 | data output; bit 3 |
| D4 | 27 | data output; bit 4 |
| D5 | 28 | data output; bit 5 |
| D6 | 29 | data output; bit 6 |
| D7 | 30 | data output; bit 7 |
| D8 | 31 | data output; bit 8 |
| n.c. | 32 | not connected |

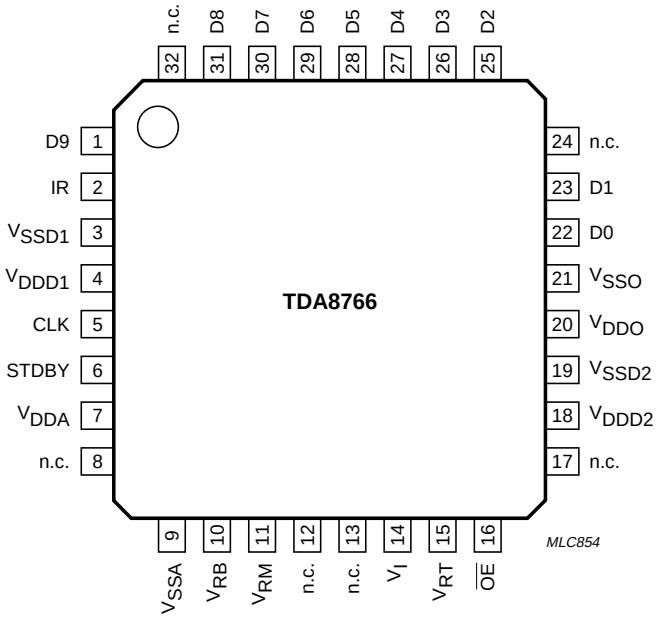



Fig.2 Pin configuration.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDA}$ | analog supply voltage | note 1 | −0.3 | +7.0 | V |
| $V_{DDD}$ | digital supply voltage | note 1 | −0.3 | +7.0 | V |
| $V_{DDO}$ | output stages supply voltage | note 1 | −0.3 | +7.0 | V |
| $\Delta V_{DD}$ | supply voltage difference | | | | |
| | $V_{DDA} - V_{DDD}$ | | −1.0 | +4.0 | V |
| | $V_{DDD} - V_{DDO}$ | | −1.0 | +4.0 | V |
| | $V_{DDA} - V_{DDO}$ | | −1.0 | +4.0 | V |
| $V_I$ | input voltage | referenced to $V_{SSA}$ | −0.3 | +7.0 | V |
| $V_{i(p-p)}$ | AC input voltage for switching (peak-to-peak value) | referenced to $V_{SSD}$ | − | $V_{DDD}$ | V |
| $I_O$ | output current | | − | 10 | mA |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| $T_{amb}$ | ambient temperature | | −20 | +75 | °C |
| $T_j$ | junction temperature | | − | 150 | °C |

**Note**

1. The supply voltages $V_{DDA}$, $V_{DDD}$ and $V_{DDO}$ may have any value between −0.3 and +7.0 V provided that the supply voltage differences $\Delta V_{DD}$ are respected.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(jj-a)}$ | thermal resistance from junction to ambient | in free air | 90 | K/W |

## CHARACTERISTICS

$V_{DDA}$ = $V_7$ to $V_9$ = 3.3 V; $V_{DDD}$ = $V_4$ to $V_3$ = $V_{18}$ to $V_{19}$ = 3.3 V; $V_{DDO}$ = $V_{20}$ to $V_{21}$ = 3.3 V; $V_{SSA}$, $V_{SSD}$ and $V_{SSO}$ short-circuited together; $V_{i(p-p)}$ = 1.83 V; $C_L$ = 20 pF; $T_{amb}$ = 0 to 70 °C; typical values measured at $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDA}$ | analog supply voltage | | 3.0 | 3.3 | 5.25 | V |
| $V_{DDD1}$ | digital supply voltage 1 | | 3.0 | 3.3 | 5.25 | V |
| $V_{DDD2}$ | digital supply voltage 2 | | 3.0 | 3.3 | 5.25 | V |
| $V_{DDO}$ | output stages supply voltage | | 3.0 | 3.3 | 5.25 | V |
| $\Delta V_{DD}$ | voltage difference | | | | | |
| | $V_{DDA} - V_{DDD}$ | | –0.2 | – | +0.2 | V |
| | $V_{DDA} - V_{DDO}$ | | –0.2 | – | +0.2 | V |
| | $V_{DDD} - V_{DDO}$ | | –0.2 | – | +0.2 | V |
| $I_{DDA}$ | analog supply current | | – | 7.5 | 10 | mA |
| $I_{DDD}$ | digital supply current | | – | 7.5 | 10 | mA |
| $I_{DDO}$ | output stages supply current | $f_{clk}$ = 20 MHz; ramp input; $C_L$ = 20 pF | – | 1 | 2 | mA |
| $P_{tot}$ | total power dissipation | operating; $V_{DD}$ = 3.3 V | – | 53 | 73 | mW |
| | | standby mode | – | 4 | – | mW |
| **Inputs** | | | | | | |
| CLOCK INPUT CLK (REFERENCED TO $V_{SSD}$); note 1 | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | – | $0.3V_{DDD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | $V_{DDD} \leq 3.6$ V | $0.6V_{DDD}$ | – | $V_{DDD}$ | V |
| | | $V_{DDD}$ = 3.3 V | $0.7V_{DDD}$ | – | $V_{DDD}$ | V |
| $I_{IL}$ | LOW-level input current | $V_{CLK} = 0.3V_{DDD}$ | –1 | 0 | +1 | µA |
| $I_{IH}$ | HIGH-level input current | $V_{CLK} = 0.7V_{DDD}$ | – | – | 5 | µA |
| $Z_i$ | input impedance | $f_{clk}$ = 20 MHz | – | 4 | – | kΩ |
| $C_i$ | input capacitance | $f_{clk}$ = 20 MHz | – | 3 | – | pF |
| INPUTS $\overline{OE}$ AND STDBY (REFERENCED TO $V_{SSD}$); see Tables 1 and 2 | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | – | $0.3V_{DDD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | $V_{DDD} \leq 3.6$ V | $0.6V_{DDD}$ | – | $V_{DDD}$ | V |
| | | $V_{DDD}$ = 3.3 V | $0.7V_{DDD}$ | – | $V_{DDD}$ | V |
| $I_{IL}$ | LOW-level input current | $V_{IL} = 0.3\ V_{DDD}$ | –1 | – | – | µA |
| $I_{IH}$ | HIGH-level input current | $V_{IH} = 0.7\ V_{DDD}$ | – | – | 1 | µA |
| ANALOG INPUT $V_I$ (REFERENCED TO $V_{SSA}$) | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I = V_{RB}$ | – | 0 | – | µA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{RT}$ | – | 35 | – | µA |
| $Z_i$ | input impedance | $f_i$ = 1 MHz | – | 5 | – | kΩ |
| $C_i$ | input capacitance | $f_i$ = 1 MHz | – | 8 | – | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Reference voltages for resistor ladder;** see Table 3 | | | | | | |
| $V_{RB}$ | reference voltage BOTTOM | | 1.1 | 1.2 | – | V |
| $V_{RT}$ | reference voltage TOP | | 3.0 | 3.3 | $V_{DDA}$ | V |
| $V_{diff(ref)}$ | differential reference voltage $V_{RT} - V_{RB}$ | | 1.9 | 2.1 | 3.0 | V |
| $I_{ref}$ | reference current | | – | 7.2 | – | mA |
| $R_{LAD}$ | ladder resistance | | – | 290 | – | Ω |
| $TC_{RLAD}$ | temperature coefficient of ladder resistance | | – | 539 | – | mΩ/K |
| | | | – | 1860 | – | ppm |
| $V_{offset(B)}$ | offset voltage BOTTOM | note 2 | – | 135 | – | mV |
| $V_{offset(T)}$ | offset voltage TOP | note 2 | – | 135 | – | mV |
| $V_{I(p-p)}$ | analog input voltage (peak-to-peak value) | note 3 | 1.66 | 1.83 | 2.35 | V |
| **Outputs** | | | | | | |
| DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO $V_{SSD}$) | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_O$ = 1 mA | 0 | – | 0.5 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_O$ = –1 mA | $V_{DDO}$ – 0.5 | – | $V_{DDO}$ | V |
| $I_{OZ}$ | output current in 3-state mode | 0.5 V < $V_O$ < $V_{DDO}$ | –20 | – | +20 | μA |
| **Switching characteristics** | | | | | | |
| CLOCK INPUT CLK; see Fig.4; note 1 | | | | | | |
| $f_{clk(max)}$ | maximum clock frequency | | 20 | – | – | MHz |
| $t_{CPH}$ | clock pulse width HIGH | | 15 | – | – | ns |
| $t_{CPL}$ | clock pulse width LOW | | 15 | – | – | ns |
| **Analog signal processing ($f_{clk}$ = 20 MHz)** | | | | | | |
| LINEARITY | | | | | | |
| INL | integral non-linearity | ramp input; see Fig.6 | – | ±1 | ±2 | LSB |
| DNL | differential non-linearity | ramp input; see Fig.7 | – | ±0.25 | ±0.7 | LSB |
| INPUT SET RESPONSE; see Fig.8; note 4 | | | | | | |
| $t_{STLH}$ | analog input settling time LOW-to-HIGH | full-scale square wave | – | 4 | 6 | ns |
| $t_{STHL}$ | analog input settling time HIGH-to-LOW | full-scale square wave | – | 4 | 6 | ns |
| HARMONICS; see Fig.9; note 5 | | | | | | |
| THD | total harmonic distortion | $f_i$ = 1 MHz | – | –63 | – | dB |
| SIGNAL-TO-NOISE RATIO; see Fig.9; note 5 | | | | | | |
| S/N | signal-to-noise ratio (full-scale) | without harmonics; $f_i$ = 1 MHz | – | 60 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| EFFECTIVE BITS; see Fig.9; note 5 | | | | | | |
| EB | effective bits | $f_i$ = 300 kHz | – | 9.5 | – | bits |
| | | $f_i$ = 1 MHz | – | 9.3 | – | bits |
| | | $f_i$ = 3.58 MHz | – | 8.0 | – | bits |
| **Timing ($f_{clk}$ = 20 MHz; $C_L$ = 20 pF);** see Fig.4; note 6 | | | | | | |
| $t_{ds}$ | sampling delay time | | – | – | 5 | ns |
| $t_h$ | output hold time | | 5 | – | – | ns |
| $t_d$ | output delay time | $V_{DDO}$ = 4.75 V | 8 | 12 | 15 | ns |
| | | $V_{DDO}$ = 3.15 V | 8 | 17 | 20 | ns |
| **3-state output delay times;** see Fig.5 | | | | | | |
| $t_{dZH}$ | enable HIGH | | – | 14 | 18 | ns |
| $t_{dZL}$ | enable LOW | | – | 16 | 20 | ns |
| $t_{dHZ}$ | disable HIGH | | – | 16 | 20 | ns |
| $t_{dLZ}$ | disable LOW | | – | 14 | 18 | ns |
| **Standby mode output delay times** | | | | | | |
| $t_{d(stb)LH}$ | standby LOW-to-HIGH transition | | – | – | 200 | ns |
| $t_{d(stb)HL}$ | start-up HIGH-to-LOW transition | | – | – | 500 | ns |

**Notes**

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 0 up to and including 1023:
   a) $V_{offset(B)}$ (offset voltage BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM ($V_{RB}$) at $T_{amb}$ = 25 °C.
   b) $V_{offset(T)}$ (offset voltage TOP) is the difference between $V_{RT}$ (reference voltage TOP) and the analog input which produces data outputs equal to 1023 at $T_{amb}$ = 25 °C.
3. In order to ensure the optimum linearity performance of such converter architecture, the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 1023 respectively) are connected to pins $V_{RB}$ and $V_{RT}$ via offset resistors $R_{OB}$ and $R_{OT}$ as shown in Fig.3.
   a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to code 1023, is $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.871 \times (V_{RT} - V_{RB})$
   b) Since $R_L$, $R_{OB}$ and $R_{OT}$ have similar behaviour with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from device to device. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.
4. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input change (square-wave signal) in order to sample the signal and obtain correct output data.

5. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8k acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to signal-to-noise ratio: S/N = EB $\times$ 6.02 + 1.76 dB.
6. Output data acquisition: the output data is available after the maximum delay time of $t_d$.

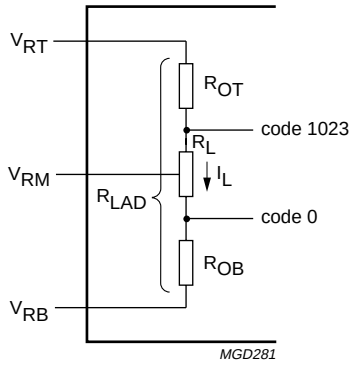



Fig.3 Converter reference resistor ladder.

**Table 1** Mode selection

| $\overline{OE}$ | D9 to D0 | IR |
|---|---|---|
| 1 | high impedance | high impedance |
| 0 | active (binary) | active |

**Table 2** Standby selection

| STDBY | D9 to D0 | $I_{DDA} + I_{DDD}$ |
|---|---|---|
| 1 | last logic state | 1.2 mA (typical value) |
| 0 | active | 15 mA (typical value) |

**Table 3** Output coding and input voltage (typical values; referenced to $V_{SSA}$)

| STEP | $V_{I(p-p)}$ | IR | BINARY OUTPUT BITS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Underflow | <1.335 V | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1.335 V | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | : | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| : | : | : | : | : | : | : | : | : | : | : | : | : |
| 1022 | : | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1023 | 3.165 V | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Overflow | >3.165 V | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

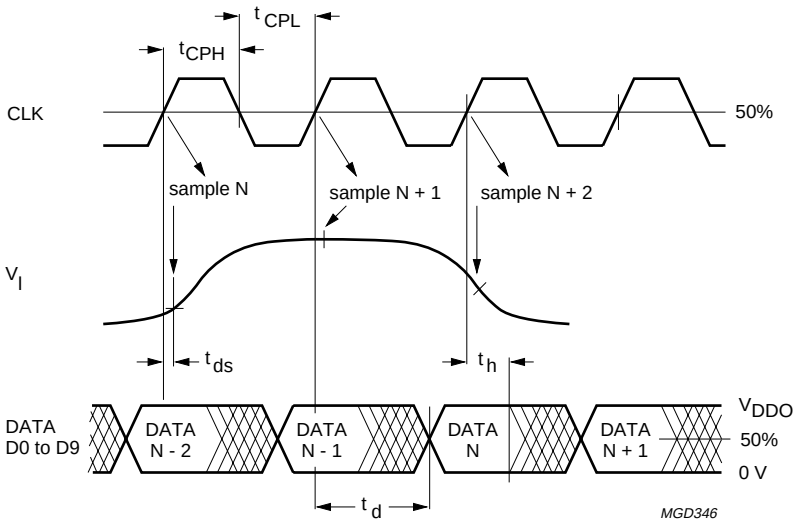
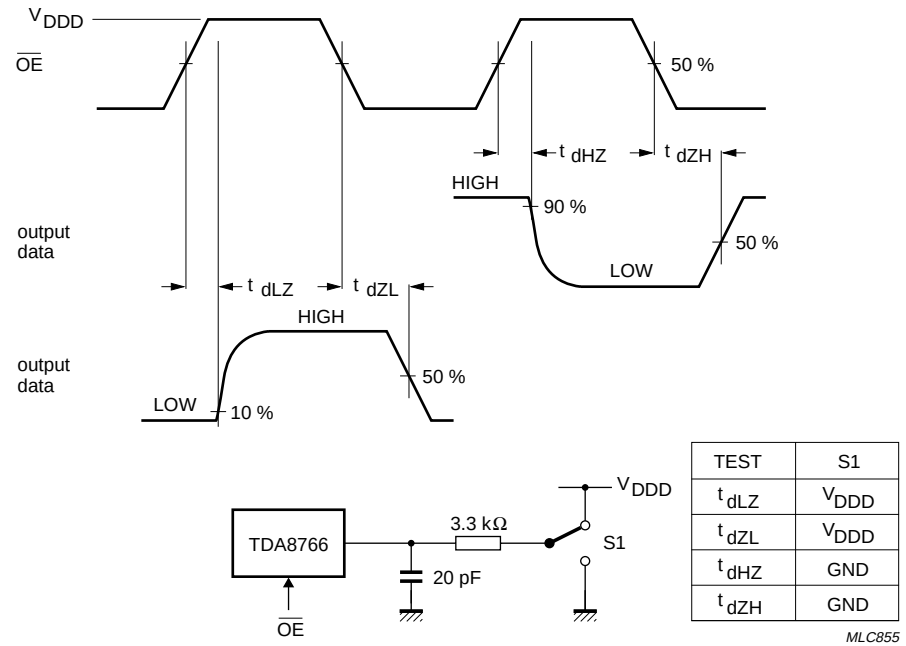



Fig.4 Timing diagram.




| TEST | S1 |
|---|---|
| $t_{dLZ}$ | $V_{DDD}$ |
| $t_{dZL}$ | $V_{DDD}$ |
| $t_{dHZ}$ | GND |
| $t_{dZH}$ | GND |

$f_{\overline{OE}}$ = 100 kHz.

Fig.5 Timing diagram and test conditions of 3-state output delay time.

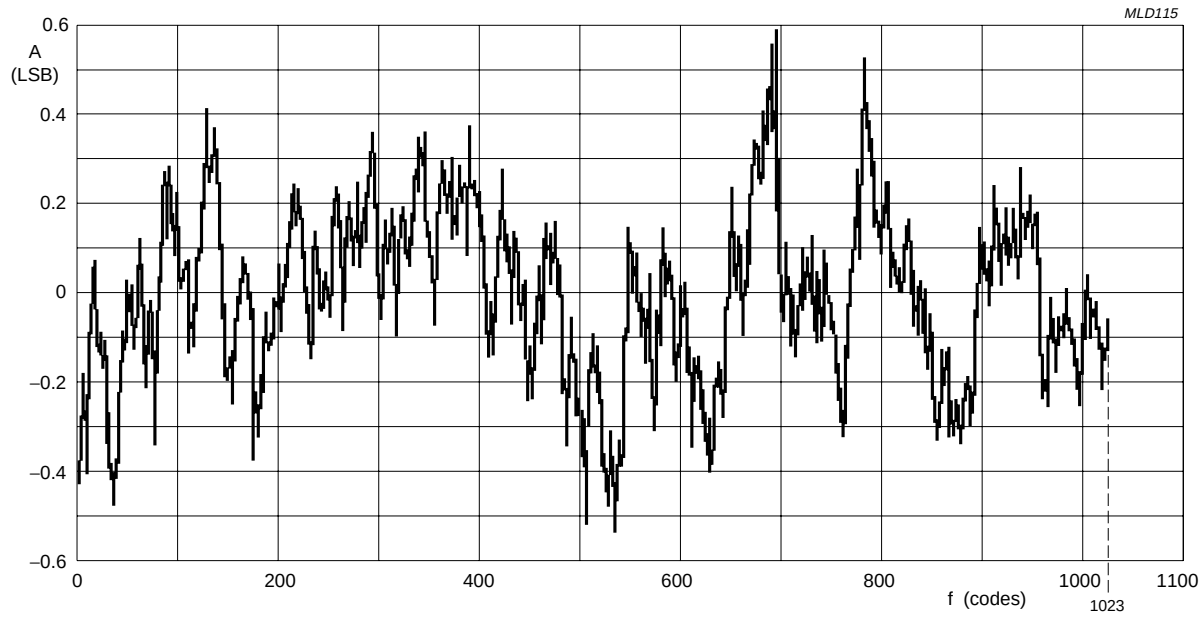



Fig.6 Typical Integral Non-Linearity (INL) performance.

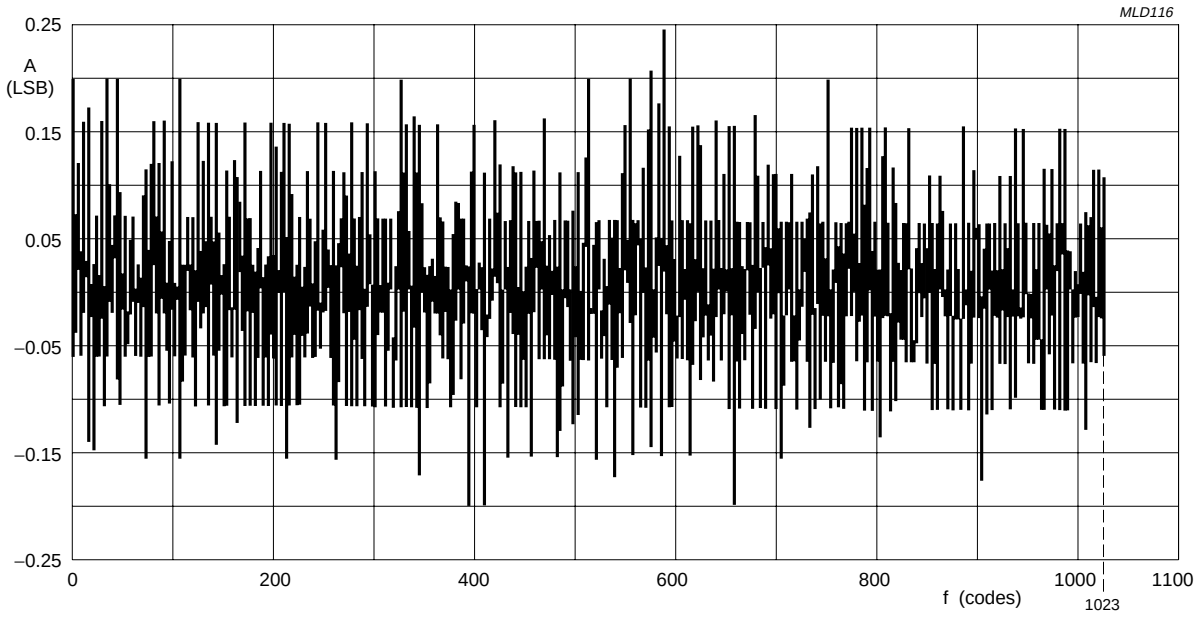



Fig.7 Typical Differential Non-Linearity (DNL) performance.

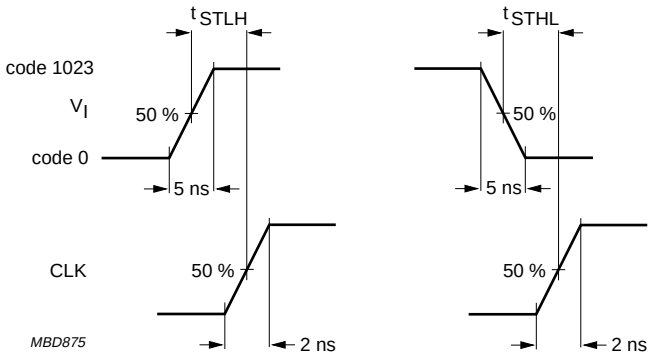
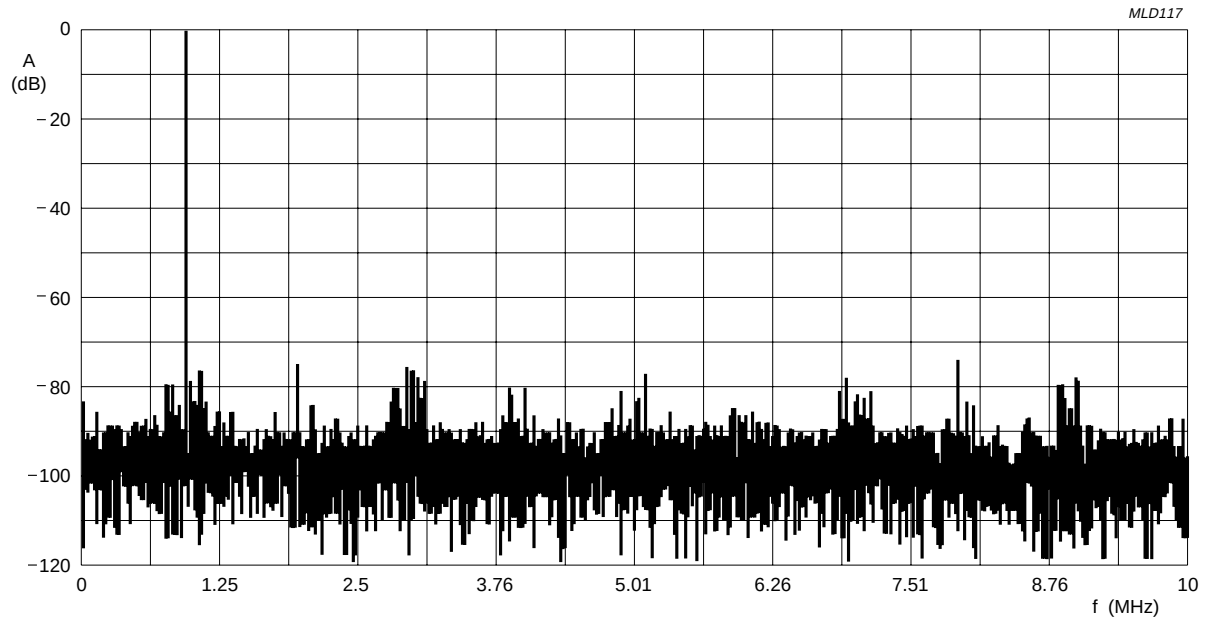



Fig.8 Analog input settling-time diagram.




Effective bits: 9.59; THD = −76.60 dB.
Harmonic levels (dB): 2nd = −81.85; 3rd = −87.56; 4th = −88.81; 5th = −88.96; 6th = −79.58.

Fig.9 Typical fast Fourier transform ($f_{clk}$ = 20 MHz; $f_i$ = 1 MHz).

## INTERNAL PIN CONFIGURATION

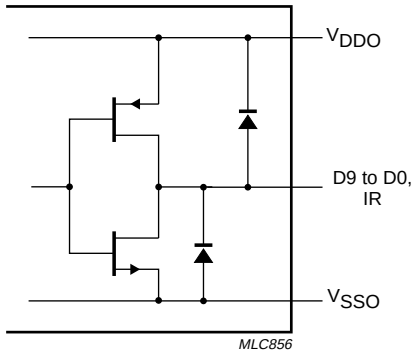



Fig.10 D9 to D0 and IR outputs.

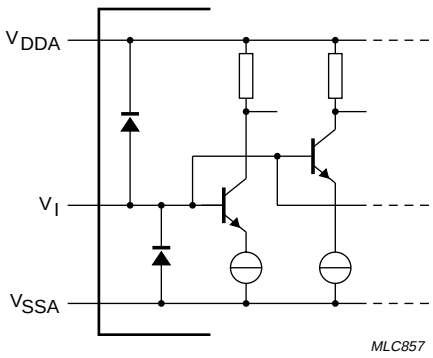



Fig.11 $V_I$ analog input.

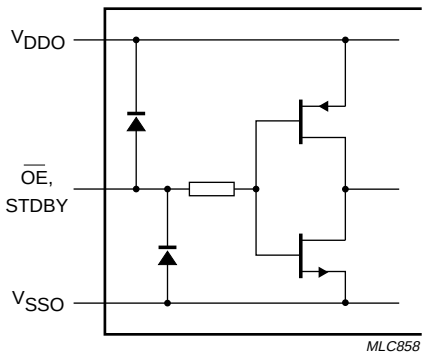



Fig.12 $\overline{OE}$ and STDBY inputs.

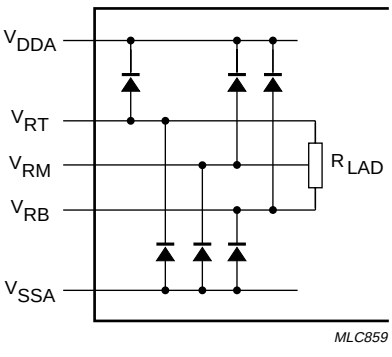



Fig.13 $V_{RB}$, $V_{RM}$ and $V_{RT}$ inputs.

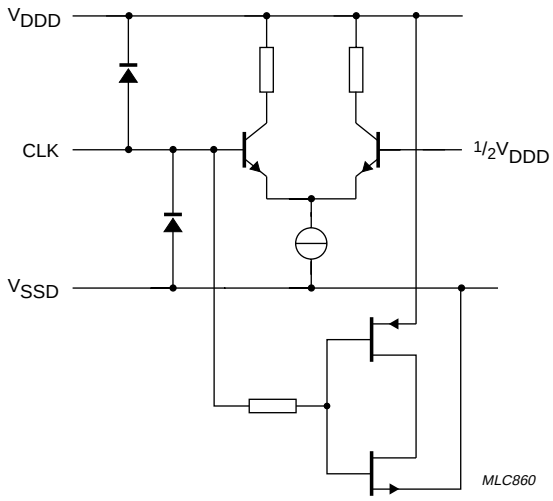
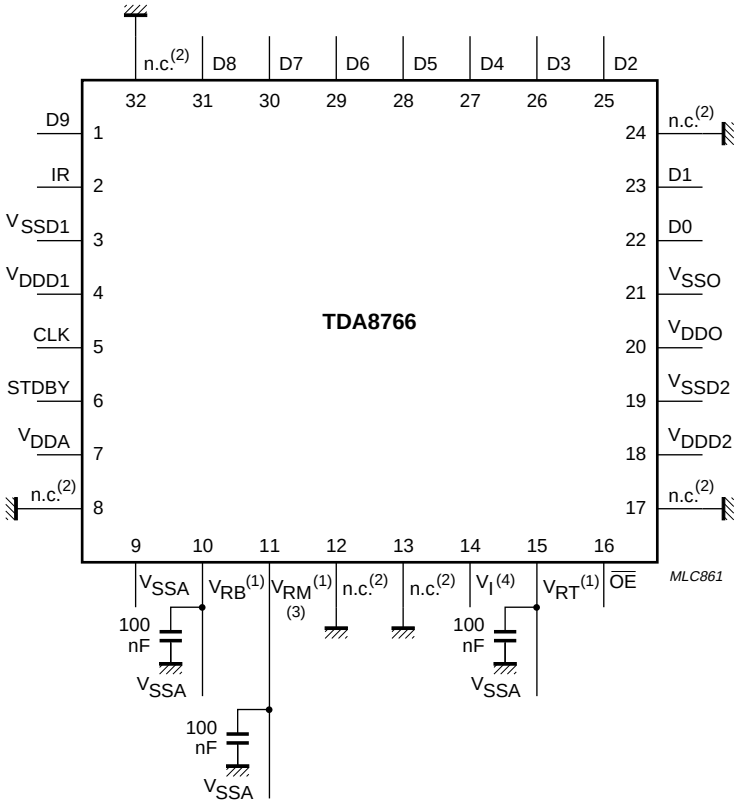



Fig.14 CLK input.

## APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number *"AN00014"*).




The analog and digital supplies should be separated and decoupled.

The external voltage reference generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated $V_{DDA}$ supply through a resistor bridge and a decoupling capacitor.

(1) $V_{RB}$, $V_{RM}$ and $V_{RT}$ are decoupled to $V_{SSA}$.

(2) Pins 8, 12, 13, 17, 24 and 32 should be connected to the closest ground pin in order to prevent noise influence.

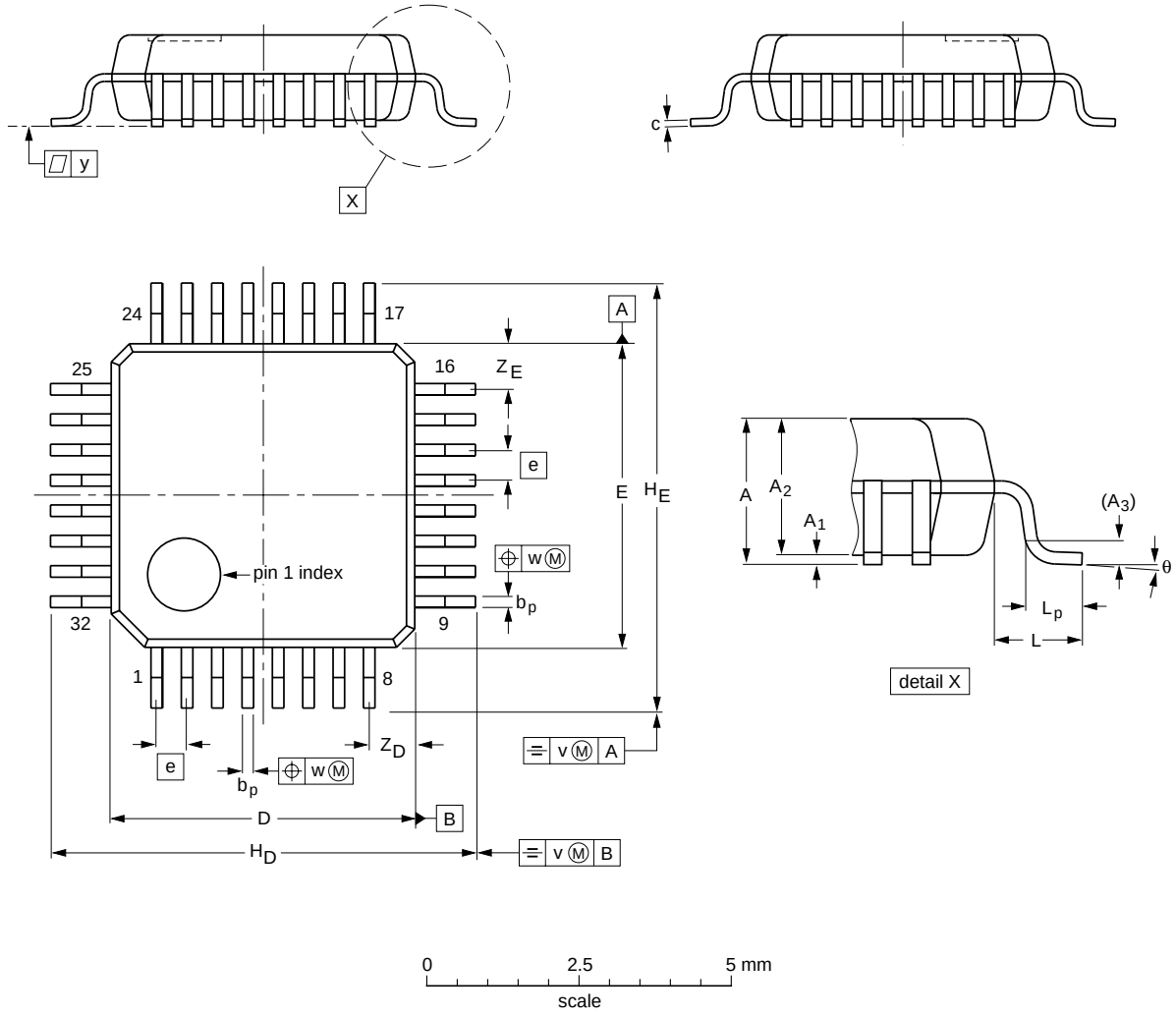
(3) When $V_{RM}$ is not used, pin 11 can be left open-circuit, avoiding the decoupling capacitor. In any case, pin 11 must not be grounded.

(4) When analog input signal is AC coupled, an input bias or a clamping level must be applied to $V_I$ input (pin 14).

Fig.15 Application diagram.

## PACKAGE OUTLINE

**LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm** **SOT401-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.15<br>0.05 | 1.5<br>1.3 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 5.1<br>4.9 | 5.1<br>4.9 | 0.5 | 7.15<br>6.85 | 7.15<br>6.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT401-1 | 136E01 | MS-026 | | | | ~~99-12-27~~<br>00-01-19 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE[1] | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW[2] |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA | not suitable | suitable |
| HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable[3] | suitable |
| PLCC[4], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[4][5] | suitable |
| SSOP, TSSOP, VSO | not recommended[6] | suitable |

**Notes**

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

**DATA SHEET STATUS**

| DATA SHEET STATUS[1] | PRODUCT STATUS[2] | DEFINITIONS |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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**Notes**

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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